RECEIVED
CENTRAL FAX CENTER
JAN 03 2007

IN THE SPECIFICATION:

Please replace the heading on page 6 line 4 with the following amended heading:

DETAILED ~~DESCRITPION~~ DESCRIPTION OF EMBODIMENTS

Please replace the ASTRACT with the following amended paragraph:

A thin film transistor (TFT) array panel includes: an insulating substrate (110); first and second semiconductor members (151 a,b) formed on the substrate and having opposite conductivity; a first gate member (121a) formed on a first layer (140), insulated from the first and the second semiconductor members and overlapping one of the first and the second semiconductor members; a second gate member (122a) formed on the [[same]] first layer (140) ~~as the first gate member (121a)~~, separated from the first gate member, and insulated from the first and the second semiconductor members (151 a,b), the second gate member (122a) not overlapping the first and the second semiconductor members; a first data member (162) formed on a second layer (160), connected to one of the first and the second semiconductor members (151 a,b) and insulated from the first (121a) and the second (122a) gate members; and a first connection (123) formed on the [[same]] second layer (160) ~~as the first data member~~ and connecting the first gate member (121a) and the second gate member (122a).

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

Please replace the paragraph on page 7 lines 4-7 with the following amended paragraph:

As shown in FIGS. 3A and 3B, a blocking layer 111 is formed on a transparent insulating substrate 110. A pair of first and second semiconductor members 151a and 151b and a pair of third and fourth semiconductor members 152a and 152b are formed on the blocking layer 111. The first and second semiconductor members 151a and 151b have opposite conductivity, while the third and fourth semiconductor members 152a and 152b also have opposite conductivity.

Please replace the paragraph on page 2 line 31 to page 3 line 4 with the following amended paragraph:

When the first gate member overlaps the first semiconductor member, the TFT array panel may further include a third gate member formed on the first layer, separated from the first and the second gate members, insulated from the first and the second semiconductor members, and overlapping the second semiconductor member and may further include a second connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the second gate member and the third gate member.

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

Please replace the paragraph on page 3 lines 5-10 with the following amended paragraph:

The TFT array panel may further include: a fourth gate member formed on the first layer, separated from the first, the second, and the third gate members and insulated from the first and the second semiconductor members, the fourth gate member not overlapping the first and the second semiconductor members; and a second connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the third gate member and the fourth gate member.

Please replace the paragraph on page 3 lines 11-19 with the following amended paragraph:

The TFT array panel may further include: fifth and sixth gate members formed on the first layer, separated from the first to the fourth gate members, insulated from the first and the second semiconductor members, and overlapping the first and the second semiconductor members, respectively; a seventh gate member formed on the first layer, separated from the first to the sixth gate members and insulated from the first and the second semiconductor members, the seventh gate member not overlapping the first and the second semiconductor members; and third and fourth connections formed on the [[same]] second layer ~~as the first data member~~ and connecting the fifth and the sixth gate members to the seventh gate member.

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

Please replace the paragraph on page 3 lines 20-22 with the following amended paragraph:

The TFT array panel may further include a fifth connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the first semiconductor member and the second semiconductor member.

Please replace the paragraph on page 3 lines 23-30 with the following amended paragraph:

The TFT array panel may further include: third and fourth semiconductor members formed on the substrate and having opposite conductivity; eighth and ninth gate members formed on the first layer, separated from the first to the seventh gate members, insulated from the first to the fourth semiconductor members, overlapping the third and the fourth semiconductor members, respectively; and sixth and seventh connections formed on the [[same]] second layer ~~as the first data member~~ and connecting the fifth and the sixth gate members to the eighth and the ninth gate members, respectively.

Please replace the paragraph on page 3 line 31 to page 4 line 8 with the following amended paragraph:

The TFT array panel may further include: tenth and eleventh gate members formed on the first layer, insulated from the first to the fourth semiconductor members and overlapping the third and the fourth semiconductor members,

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

respectively; twelfth and thirteenth gate members formed on the [[same]] first layer ~~as the tenth and the eleventh gate members~~, separated from the first to the eleventh gate members, and insulated from the third and the fourth semiconductor members, the twelfth and the thirteenth gate members not overlapping the first to the fourth semiconductor members; and eighth and ninth connections formed on the [[same]] second layer ~~as the first data member~~ and connecting the tenth and the eleventh gate members to the twelfth and the thirteenth gate members, respectively.

Please replace the paragraph on page 4 lines 9-11 with the following amended paragraph:

The TFT array panel may further include a seventh connection formed on the [[same]] second layer ~~as the first data member~~ and connecting the third semiconductor member and the fourth semiconductor member.

Please replace the paragraph on page 4 line 27 to page 5 line 14 with the following amended paragraph:

A method of manufacturing a thin film transistor (TFT) array panel is provided, which includes: forming a blocking layer on a substrate; depositing an amorphous silicon film on the blocking layer; crystallizing the amorphous silicon film into a polysilicon film; patterning the polysilicon film to form first and second polysilicon members; forming a gate

LAW OFFICES OF MACPHERSON KWOK CHEN & HEID LLP
2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

insulating layer on the first and the second polysilicon members; forming a plurality of first conductive members overlapping the first and the second polysilicon members; [[and]] forming a plurality of second conductive members not overlapping the first and the second polysilicon members; implanting N type impurity to form a plurality of N type impurity regions in the first polysilicon member; implanting P type impurity to form a plurality of P type impurity regions in the second polysilicon member; depositing an interlayer insulating layer on the first and the second conductive members and the N type and the P type impurity regions; patterning the interlayer insulating layer and the gate insulating layer to form a plurality of first contact holes exposing portions of the first and the second conductive members and to form a plurality of second contact holes exposing portions of the N type and the P type impurity regions; [[and]] forming a plurality of connections connected to the first and the second conductive members through the first contact holes; and forming a plurality of data members connected to the N type and the P type impurity regions through the second contact holes.

Please replace the paragraph on page 5 lines 17-20 with the following amended paragraph:

The data members may include first and second voltage ~~supplying~~ lines respectively connected to the N type and the P

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP
2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

type impurity regions for transmitting first and second voltages; and[[/or]] may include a connecting member connected to both the N type impurity region and the P type impurity region.

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049